Our Docket No.: 042390.P10571

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Blaise B. Fanning et al.

Application No.: **09/823,126**

Filed: **March 30, 2001**

For: **PREFETCH CANCELLATION THROUGH KNOWLEDGE OF SYSTEM CACHING POLICY**

Examiner:

Art Group:

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231-9999

Sir:

Prior to the examination on the merits of the instant application, please consider the following amendments.

AMENDMENTS

In the Claims

A clean version of the entire set of pending claims as amended by this Response is presented on the following page.

Claims 8, 18, 20, and 28 are amended as indicated by a marked up version of the rewritten claims, which follows the remarks, showing all the changes relative to the previous version of the claims:

Clean Version of the Entire Set of Pending Claims

1. An apparatus comprising:

a storage circuit coupled to a prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer.

2. The apparatus of claim 1 wherein the storage circuit comprises:

a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

3. The apparatus of claim 2 wherein the queue comprises:

a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

4. The apparatus of claim 3 wherein the canceler comprises:

a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

5. The apparatus of claim 4 wherein the canceler further comprises:

a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

6. The apparatus of claim 4 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

7. The apparatus of claim 4 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

8. (Amended) The apparatus of claim 5 wherein the cancel generator comprises:

a comparator combiner coupled to the comparators to combine the comparison results, the combined comparison results corresponding to the cancellation request.

9. The apparatus of claim 2 wherein the canceler comprises:

a matching circuit having an argument register to store the current prefetch address for matching with entries of the CAM.

10. The apparatus of claim 9 wherein the canceler further comprises:

a cancellation generator to generate a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

11. A method comprising:

storing a plurality of prefetch addresses in a storage circuit, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

canceling the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer.

12. The method of claim 11 wherein storing comprises:

storing the plurality of prefetch addresses in one of a queue with a predetermined size and a content addressable memory (CAM).

13. The method of claim 12 wherein storing the plurality of prefetch addresses in the queue comprises:

storing the plurality of prefetch addresses in a plurality of registers cascaded to shift the prefetch addresses each time the processor generates a prefetch request.

14. The method of claim 13 wherein canceling comprises:

matching a current prefetch address associated with the access request with the stored prefetch addresses.

15. The method of claim 14 wherein canceling further comprises:

generating a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

16. The method of claim 14 wherein matching comprises:

comparing the current prefetch address with each of the stored prefetch addresses.

17. The method of claim 14 wherein matching comprises:

comparing the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

18. (Amended) The method of claim 15 wherein generating the cancellation request comprises:

combining the comparison results, the combined comparison results corresponding to the cancellation request.

19. The method of claim 12 wherein canceling comprises:

storing the current prefetch address in an argument register for matching with entries of the CAM.

20. (Amended) The method of claim 19 wherein canceling further comprises:

generating a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

21. A system comprising:

a processor to generate prefetch requests;

a memory to store data; and

a chipset coupled to the processor and the memory, the chipset comprising:

a prefetcher to generate an access request to the memory when requested by the processor;

a prefetch monitor circuit coupled to the prefetcher, the prefetch monitor circuit comprising:

a storage circuit coupled to the prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer.

22. The system of claim 21 wherein the storage circuit comprises:

a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

23. The system of claim 22 wherein the queue comprises:

a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

24. The system of claim 23 wherein the canceler comprises:

a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

25. The system of claim 24 wherein the canceler further comprises:

a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

26. The system of claim 24 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

27. The system of claim 24 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

28. (Amended) The system of claim 25 wherein the cancel generator comprises:

a comparator combiner coupled to the comparators to combine the comparison results, the combined comparison results corresponding to the cancellation request.

29. The system of claim 22 wherein the canceler comprises:

a matching circuit having an argument register to store the current prefetch address for matching with entries of the CAM.

30. The system of claim 29 wherein the canceler further comprises:

a cancellation generator to generate a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

REMARKS

This Preliminary Amendment is filed prior to receipt of an Office Action. Upon review, Applicant became aware of typographical errors in claim dependency numbering. Each voluntary amendment to correct a typographical error neither narrows the scope of that claim nor addresses issues related to statutory grounds for patentability.

Version With Markings to Show Changes Made

In the Claims

1. An apparatus comprising:

a storage circuit coupled to a prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer.

2. The apparatus of claim 1 wherein the storage circuit comprises:

a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

3. The apparatus of claim 2 wherein the queue comprises:

a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

4. The apparatus of claim 3 wherein the canceler comprises:

a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

5. The apparatus of claim 4 wherein the canceler further comprises:

a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

6. The apparatus of claim 4 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

7. The apparatus of claim 4 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

8. (Amended) The apparatus of claim [7] 5 wherein the cancel generator comprises:

a comparator combiner coupled to the comparators to combine the comparison results, the combined comparison results corresponding to the cancellation request.

9. The apparatus of claim 2 wherein the canceler comprises:

a matching circuit having an argument register to store the current prefetch address for matching with entries of the CAM.

10. The apparatus of claim 9 wherein the canceler further comprises:

a cancellation generator to generate a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

11. A method comprising:

storing a plurality of prefetch addresses in a storage circuit, the plurality of prefetch addresses corresponding to most recent

access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

canceling the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer.

12. The method of claim 11 wherein storing comprises:

storing the plurality of prefetch addresses in one of a queue with a predetermined size and a content addressable memory (CAM).

13. The method of claim 12 wherein storing the plurality of prefetch addresses in the queue comprises:

storing the plurality of prefetch addresses in a plurality of registers cascaded to shift the prefetch addresses each time the processor generates a prefetch request.

14. The method of claim 13 wherein canceling comprises:

matching a current prefetch address associated with the access request with the stored prefetch addresses.

15. The method of claim 14 wherein canceling further comprises:

generating a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

16. The method of claim 14 wherein matching comprises:

comparing the current prefetch address with each of the stored prefetch addresses.

17. The method of claim 14 wherein matching comprises:

comparing the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

18. (Amended) The method of claim [17] 15 wherein generating the cancellation request comprises:

combining the comparison results, the combined comparison results corresponding to the cancellation request.

19. The method of claim 12 wherein canceling comprises:

storing the current prefetch address in an argument register for matching with entries of the CAM.

20. (Amended) The method of claim [9] 19 wherein canceling further comprises:

generating a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

21. A system comprising:

a processor to generate prefetch requests;

a memory to store data; and

a chipset coupled to the processor and the memory, the chipset comprising:

a prefetcher to generate an access request to the memory when requested by the processor;

a prefetch monitor circuit coupled to the prefetcher, the prefetch monitor circuit comprising:

a storage circuit coupled to the prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer.

22. The system of claim 21 wherein the storage circuit comprises:

a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

23. The system of claim 22 wherein the queue comprises:

a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

24. The system of claim 23 wherein the canceler comprises:

a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

25. The system of claim 24 wherein the canceler further comprises:

a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

26. The system of claim 24 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

27. The system of claim 24 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

28. (Amended) The system of claim [27] 25 wherein the cancel generator comprises:

a comparator combiner coupled to the comparators to combine the comparison results, the combined comparison results corresponding to the cancellation request.

29. The system of claim 22 wherein the canceler comprises:

a matching circuit having an argument register to store the current prefetch address for matching with entries of the CAM.

30. The system of claim 29 wherein the canceler further comprises:

a cancellation generator to generate a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

Conclusion

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for examination, and such action is respectfully solicited at the Examiner's earliest conveneince.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: May 29, 2001

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on: May 29, 2001.

5/29/01

Eric Hoover   Date